What is claimed is:

1. A gain amplifier with DC offset cancellation circuit comprising:

a gain amplifier, having an input end coupled to an input signal source;

a buffer, having an input end coupled to the output end of the gain amplifier; and

an active low-pass analogue filter, coupled to the output end of the buffer, for filtering input analogue signals at high frequencies, and feeding the filtered buffer output signals to the input end of gain amplifier to be deducted from the input signals, so as to cancel DC bias.

2. The gain amplifier with DC offset cancellation circuit of claim 1, wherein the active low-pass analogue filter having a variable resistor, an amplifier, a capacitor pair and a comparator, the amplifier being coupled to the output of the variable resistor, a negative feedback being provided from the output of the variable resistor to the input signal source, the capacitor pair being coupled to the amplifier, one input of the comparator

being coupled to the output of the amplifier, the other input of the comparator being coupled to a reference voltage source, signals being output to the variable resistor after comparing with the reference voltage in the comparator.

3. The gain amplifier with DC offset cancellation circuit of claim 1, wherein the variable capacitor comprises a plurality of metallic oxide semiconductor field effect transistors (MOSFETs).

4. The gain amplifier with DC offset cancellation circuit of claim 1, wherein the gates of said plurality of MOSFETs are coupled to the output of the comparator, the sources of said plurality of MOSFETs are coupled to both output ends of the buffer, and the drains of said plurality of MOSFETs are output to the amplifier for controlling output voltage.